# Superlattice Nanowire Pattern Transfer (SNAP)

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## CONSPECTUS

**D**uring the past 15 years or so, nanowires (NWs) have emerged as a new and distinct class of materials. Their novel structural and physical properties separate them from wires that can be prepared using the standard methods for manufacturing electronics. NW-based applications that range from traditional electronic devices (logic and memory) to novel biomolecular and chemical sensors, thermoelectric materials, and optoelectronic devices, all have appeared during the past few years. From a fundamental perspective, NWs provide a route toward the investigation of new physics in confined dimensions.



Perhaps the most familiar fabrication method is the vapor−liquid−solid (VLS) growth technique, which produces semiconductor nanowires as bulk materials. However, other fabrication methods exist and have their own advantages.

In this Account, I review a particular class of NWs produced by an alternative method called superlattice nanowire pattern transfer (SNAP). The SNAP method is distinct from other nanowire preparation methods in several ways. It can produce large NW arrays from virtually any thin-film material, including metals, insulators, and semiconductors. The dimensions of the NWs can be controlled with near-atomic precision, and NW widths and spacings can be as small as a few nanometers. In addition, SNAP is almost fully compatible with more traditional methods for manufacturing electronics. The motivation behind the development of SNAP was to have a general nanofabrication method for preparing electronics-grade circuitry, but one that would operate at macromolecular dimensions and with access to a broad materials set. Thus, electronics applications, including novel demultiplexing architectures; large-scale, ultrahigh-density memory circuits; and complementary symmetry nanowire logic circuits, have served as drivers for developing various aspects of the SNAP method. Some of that work is reviewed here.

As the SNAP method has evolved into a robust nanofabrication method, it has become an enabling tool for the investigation of new physics. In particular, the application of SNAP toward understanding heat transport in low-dimensional systems is discussed. This work has led to the surprising discovery that Si NWs can serve as highly efficient thermoelectric materials. Finally, we turn toward the application of SNAP to the investigation of quasi-one-dimensional (quasi-1D) superconducting physics in extremely high aspect ratio Nb NWs.
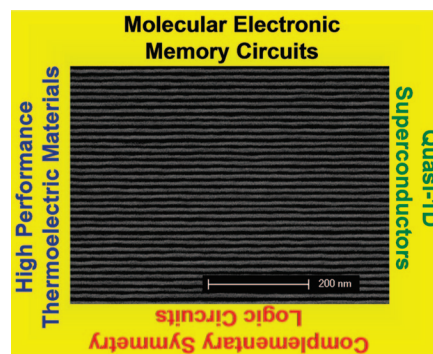
## Introduction

Many metal and semimetal nanowires (NWs) can be prepared by electrochemically depositing the NW materials into the vertically aligned pores of an anodically etched alumina film.[1] Most semiconductor NWs[2] are produced using the vapor−liquid−solid (VLS) growth method that has been generalized and expanded to a host of semiconductor materials by Lieber's group.[3] VLS NWs require a metal nanoparticle to seed NW growth, and NWs are often prepared as a powder or as a surface-supported film. While some parameters, such as the concentration of dopants or the NW length, are difficult to control, novel materials, such as core−shell[4,5] or branched[6] NWs, can be prepared. Both the alumina-templated and the VLS-synthesized NWs can be prepared with an alternating and controllable stoichiometry along
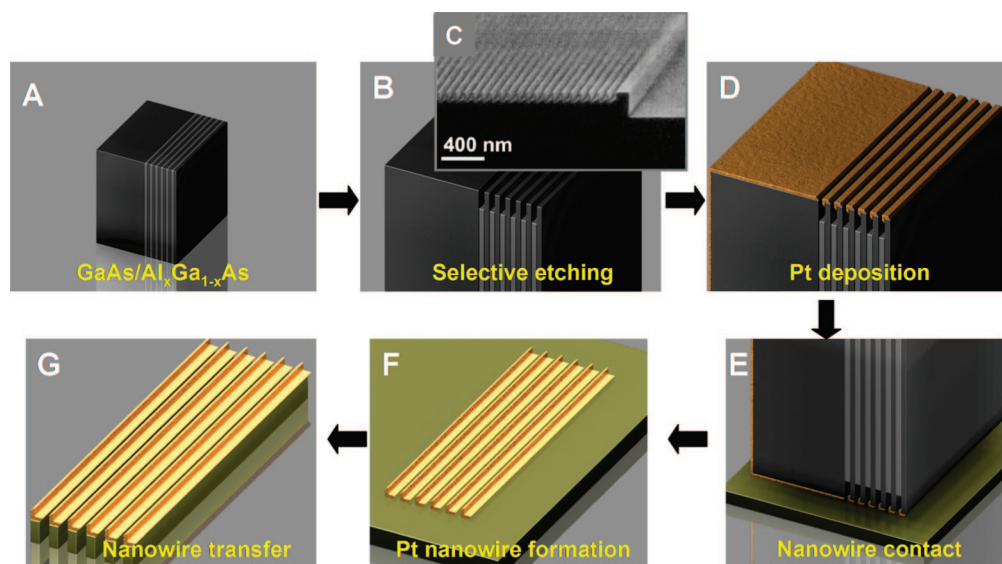
**FIGURE 1.** The SNAP process: (A) A piece of a GaAs/Al$_x$Ga$_{1-x}$As superlattice serves as the master. (B) The superlattice is differentially etched, leaving a comb-like structure. (C) A SEM micrograph of an etched master is shown. (D) Metal (typically Pt) is evaporated onto the master. (E) The master is dropped onto a substrate precoated with a thin epoxy layer. (F) The interface between the evaporated metal and the superlattice is etched, leaving nanowires on the surface. (G) Dry etching translates the metal nanowire array into the supporting substrate.

the long axis of the NW.[7] Most NWs are studied for their electronic (or optoelectronic) properties.[8] These classes of NWs need to be organized into the desired device setting and that remains a challenge. Thus, the majority of NW studies have focused on single or few-device demonstrations, albeit often with spectacular resulting science.

The superlattice nanowire pattern transfer method, or SNAP,[9] provides an alternative to these materials methods, with its own unique advantages. Namely, SNAP can be harnessed to produce large arrays of virtually any type of NW; the only limitation is that the material from which the NWs are made must begin as a thin film. The SNAP technique resides between NW materials growth methods (the template for SNAP NWs is grown) and traditional top-down patterning methods. Figure 1 presents a flow diagram of the SNAP process.

SNAP NWs have other advantages. First they inherit their doping levels, stoichiometry, crystallographic orientation, and thickness from the thin film substrate from which they are made. This means, for example, that p-type and n-type Si NWs can be readily prepared side by side and that pn diodes and other devices are readily obtained. Some NW materials are uniquely available using SNAP, including insulators and certain metals.

Second, the width and pitch of an array of SNAP NWs are translated from the precisely controlled film thicknesses and spacings of the superlattice template (Figure 1A). Arrays containing $10^3$ or more nontouching, well-conducting NWs with

NW widths as thin as $7 \pm 2$ nm and at a NW array pitch of $13 \pm 2$ nm have been prepared. No other method can approach these dimensions with such precision.

Third, SNAP NWs may be a millimeter long or longer. Materials grown NWs typically have lengths of 10 $\mu$m or less. Long NWs can exhibit unique physics, and they enable the construction of relatively large scale NW circuits.

In this Account, I will first discuss the SNAP fabrication method, and the ultrahigh density electronics applications that drove its development, before turning toward some of the new physics that we are exploring with SNAP NWs.

## The SNAP Fabrication Process

The process for producing SNAP NW arrays is illustrated in Figure 1. The process details are published elsewhere,[9,10] so only the most salient points are presented here. First, a custom-grown Al$_x$Ga$_{1-x}$As/GaAs superlattice is cleaved into 2 mm wide × 5 mm long "masters" (Figure 1A). One of the 2 mm wide edges is an atomically flat {110} or {100} plane. A comb-like structure (Figure 1B,C) is generated by differentially etching the superlattice using a dilute NH$_4$OH/H$_2$O$_2$/H$_2$O etch solution. Pt metal is then deposited onto the superlattice edge at an angle that varies from 15° to 45°, depending upon the pitch of the superlattice (Figure 1D). Those Pt NWs are then transferred as an ink by gently dropping them onto a substrate coated with a thin (10 nm) layer of heat-curable epoxy (Figure 1E). The epoxy coats the thin film from which the final NWs will emerge. This dropping step may be controlled to a
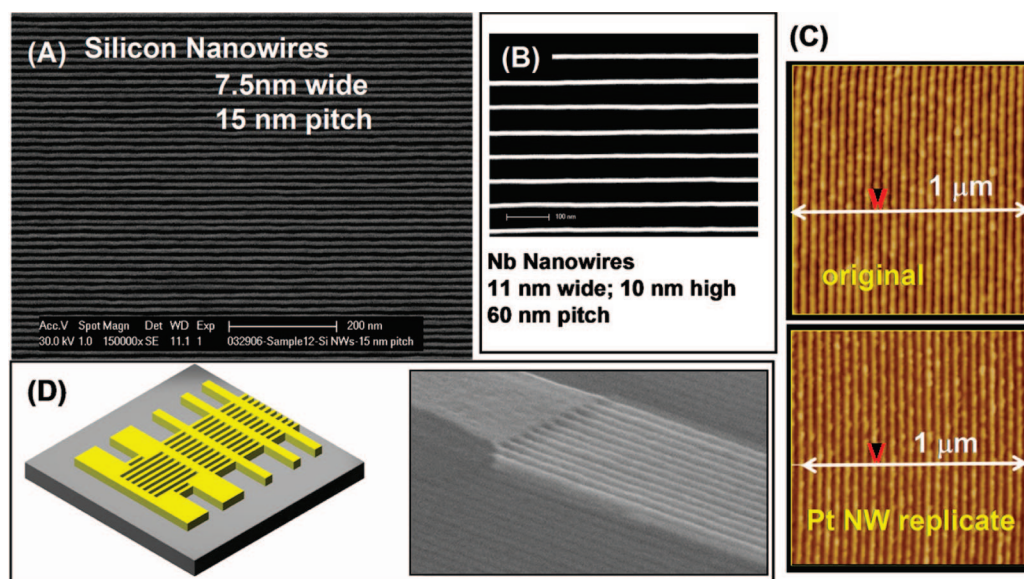
**FIGURE 2.** SNAP nanowire arrays: (A) Si NWs. These arrays are 2−3 mm long and can contain >$10^3$ NWs. (B) Nb NWs. (C) Replicating SNAP NWs via nanoimprinting. (D) Ohmic contacts to SNAP NWs can be established by carrying out additional patterning on the SOI substrate prior to the development of the NW pattern. The drawing is of a single-crystal structure consisting of a NW array plus relatively large electrical contacts. The SEM image at right shows this type of structure for Si NWs.

spatial accuracy of ±1 $\mu$m using a custom-built chuck. The epoxy formulation (Epoxy Bond 110; Allied Tech Products, Ranch Dominguez, CA; 10 drops part A to 1 drop part B + 0.15 g of 6% poly(methyl methacrylate) (PMMA) in 20 mL chlorobenzene) is critical for ensuring a high process yield. The epoxy/master is heat cured, and the metal NWs are released from the superlattice using a wet chemical etch, thus forming an array of Pt NWs (Figure 1F).

The Pt NW array may be pattern-transferred, via reactive ion etching (RIE), thus converting the underlying thin film into a NW array (Figure 1G). For Si NWs, this film is typically a 20 nm thick single-crystal Si(100) epilayer of a silicon-on-insulator (SOI) wafer (Si(100)$_{SOI}$). We have also fabricated NWs from metal,[11] insulator, and multilayer thin films.[12] (Figure 2).

For the fabrication of crossbar circuits,[9,12] a second set of SNAP NWs is deposited at right angles to the first set. For other applications, NW-to-NW routing pathways or relatively large NW contacts are required.[11,13−15] In such cases, lithography may be carried out on the Pt NW/epoxy film prior to the RIE step, so that after etching, the contacts, routing structures, etc., all lie within same thin single-crystal film (Figure 2D).[16]

A one-day/one-person fabrication run can generate 10−20 high-quality NW arrays, with each array containing between $10^2$ and $10^3$ 1−2 mm long NWs. SNAP NW arrays may also be replicated using nanoimprinting[17] (Figure 2C), implying the potential for high-throughput manufacturing.

## SNAP Patterned Silicon Nanowires

A priority has been to develop high-quality Si NW arrays, since Si NWs are versatile with applications to electronics, (bio)molecular sensors,[18−20] quantum physics,[15] and thermoelectrics.[14] Each application has different requirements. For memory circuits, long, continuous, and highly conducting NWs are needed. For logic, p- and n-type NWs need to be fabricated side-by-side, the NW source-drain channels need to be lightly doped, and ohmic contacts need to be established to ends of the NWs. For all applications, surface chemistry issues are important. For thermoelectrics, the integration of p- and n-type NWs onto a platform that can efficiently funnel heat is required.[21] Thus, we discuss SNAP Si NWs in detail, although much of this discussion translates to other NW types.

**Doping Si NWs.** A figure of merit of NW quality is the NW electrical conductivity ($\sigma$) divided by that of the thin SOI epilayer film from which the NWs are patterned. Ideally, this value ($\sigma_{NW}/\sigma_B$) is 1. However, because the NWs are nearly one-dimensional conductors, charge carriers passing through the NW will unavoidably scatter off of lattice defects, surface states, etc., all of which can lower $\sigma_{NW}/\sigma_B$. We found that Si NWs fabricated from Si(100)$_{SOI}$ epilayers, doped via ion implantation, exhibited $\sigma_{NW}/\sigma_B$ values near 1 for NWs above ~40 nm in width. For NW widths ≤20 nm, $\sigma_{NW}/\sigma_B$ was 0.01−0.001.[10] For 15−20 nm wide Si NWs patterned from MBE-grown (defect-free) SOI, $\sigma_{NW}/\sigma_B$ =1. Thus, ion implantation doping leaves defects that lower $\sigma_{NW}$ when the physical dimensions
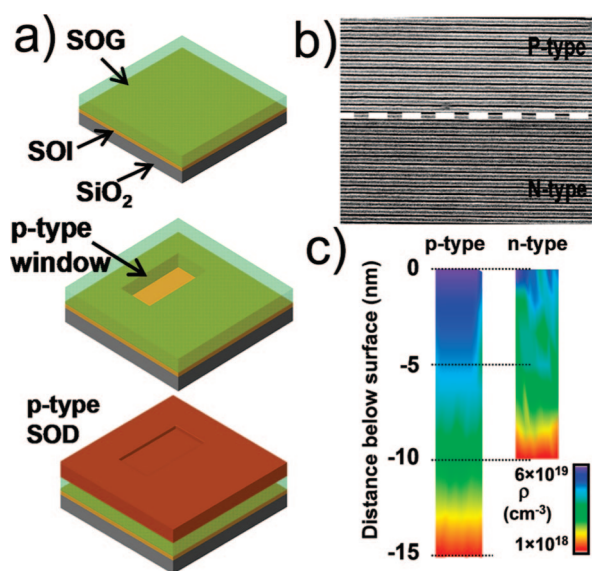
FIGURE 3. Spin-on-doping to produce p- and n-type Si NWs: (a) Fabrication steps. The SOI wafer is coated with a spin-on-glass (SOG). A window is opened in the SOG, and the wafer is coated with a spin-on-dopant film for p-type dopants, which are then are diffused into the substrate using rapid thermal annealing. The steps are repeated for n-type doping. (b) p- (top) and n-type (bottom) Si NWs in an array of 16 nm wide, 33 nm pitch Si NWs. (c) The measured dopant concentration ($\rho$) as a function of depth through the SOI film.
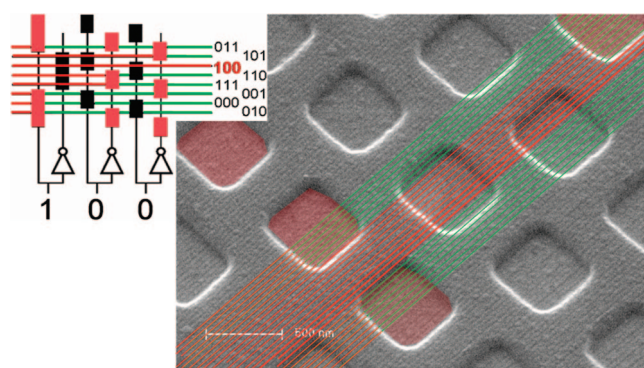


FIGURE 4. Demultiplexing concept and false-color graphic of a SNAP NW array patterned at 33 nm pitch. The top left architectural drawing shows $n = 3$ input address wire pairs demultiplexing $2^n$ (=8) NWs. The black and red bars represent regions over the NWs where a gate voltage may be applied. When a wire is gated (red bar), that wire becomes highly resistive and so is deselected (symbolized by turning green). Only one NW is selected (colored red for its entire length). The size and spacing of the bars is larger than that of the NWs, yet the address "100" still selects a single NW. The micrograph is of a SNAP NW demultiplexer following patterning of the gate regions and dielectric film deposition but prior to the deposition of the gate electrodes. The false color demonstrates an operation analogous to the architectural drawing. This demultiplexer worked. The structure of the SNAP Si NW array is visible as ridges in the gray dielectric film.

of the NW are reduced so that charge carriers passing through the NW could scatter off those defects.

We developed a gentle doping technique for SNAP Si NWs using spin-on-dopants (SOD), followed by thermal annealing to diffuse the dopants into the Si epilayer (Figure 3).[10,22] The temperature and duration of the thermal anneal determines the level and distribution of dopants through the thickness of the Si epilayers. Si NWs of width $\geq 15$ nm exhibited $\sigma_{NW}/\sigma_B$ values near 1 when prepared from SOD doped SOI. Surface scattering apparently reduces $\sigma_{NW}/\sigma_B$ values for 10 nm and smaller NWs to ~0.1.[14] P- and n-type Si NWs can be fabricated within the same array.[23]

**Ohmic Contacts to Si NWs.** Electrical contacts to highly doped (metallic) Si NWs are almost always ohmic, meaning that the current−voltage response is linear (it follows Ohm's law). For lightly doped NWs, ohmic contacts are difficult to achieve. A traditional solution for Si field effect transistors (FETs) is to highly dope the Si structure in the regions to be electrically contacted and to lightly dope the region between the contacts (the source-drain channel). This is challenging to achieve in materials grown NWs but is straightforward for SNAP NWs.[16] Note from Figure 3c that, even for highly doped NWs, the dopant concentration rapidly decreases as the top 10−15 nm of the NWs are removed. Thus for heavily doped Si NWs, ohmic metal contacts to the NWs can be established,

and those contacts can serve as etch masks while the source-drain channel is thinned. This provides a general solution for obtaining ohmic contacts to both n- and p-type NWs that are larger than ~15 nm in width. For 10 nm and thinner NWs, this approach is combined with the process illustrated in Figure 2D to establish large-area NW contacts out of the same Si single crystal from which the NWs are formed.

## Applications of SNAP to Electronic Devices

**Demultiplexing.** A modern microprocessor chip contains ~$10^8$ transistors, yet only ~$10^2$ connections to the outside world. A key element in reducing a vast number of devices to a small number of input/output wires is a demultiplexer, which is a circuit designed to separate two or more combined signals. The ultrahigh density NW arrays achievable via SNAP beg the question of whether it is possible to electrically address every individual NW using a relatively small number of microwires. Architectural concepts for meeting this challenge should bridge from the submicrometer dimensions of standard lithography to the few nanometer dimensions achievable through patterning methods like SNAP, with a few large wires addressing many NWs. NW demultiplexing concepts that are based upon binary tree demultiplexers (demux, see the drawing of Figure 4 for an example) have been proposed.[24,25] These architectures utilize $\alpha[\log_2(N)] + \beta$ large
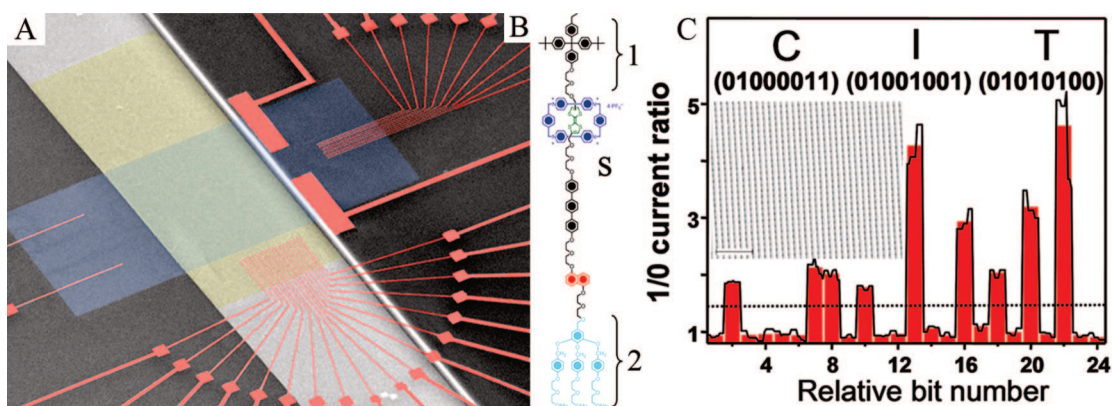
**FIGURE 5.** An ultrahigh density 160 kilobit molecular electronic memory. (A) False-color SEM micrograph of the memory is shown at left. A 400 SNAP Si NW array runs diagonally from the bottom right. These are crossed by an array of 400 Ti NWs, shown in blue. Electrical contacts for testing are shown in red. (B) The bistable, electrochemically switchable, amphiphilic [2]rotaxane, a monolayer of which is sandwiched between the top and bottom electrodes. Hydrophobic and hydrophilic stoppers are labeled 1 and 2. The switching components (labeled S) consist of a tetracationic cyclophane ring (blue) encircling either a tetrathiafulvalene group (green) (low conductance, or "0" state) or a dioxynapthyl group (red) (high conductance, or "1" state). (C) ASCII character read and write memory demonstration. The fraction of this memory that was tested is approximately shown in the inset micrograph of the crossbar. The scale bar is 200 nm.

wires to address $N$ NWs. In the most efficient case, $\alpha = 2$ and $\beta = 0$, although disordered or broken NWs require schemes with larger $\alpha$ and $\beta$ values. We reported on an efficient demux architecture and demonstration (Figure 4) that took advantage of the regular pitch and width of the NWs within a SNAP NW array.[22] It also took advantage of the doping gradient within the Si NWs to establish ohmic contacts to NWs that could be field-gated by the demux address lines.

**Ultrahigh Density Memory Circuits.** Crossbar circuits, which are formed from two crossed arrays of wires, with storage or switching elements located at the crossing junctions, have advantages[26] that have made them nanoelectronics prototypes.[25] The crossbar is simple, is defect tolerant, and is the densest electronically addressed circuit architecture for which each bit may be individually addressed.

A disadvantage of crossbars is that every bit within a crossbar is electronically connected to every other bit. A 1 or 0 state is written using a voltage, $V_W$, that is split into $\pm^1/_2V_W$ between the two crossed wires that define a bit. This means that many bits are exposed to $^1/_2V_W$, and a field-switchable junction, such as one based upon the poling of a ferroelectric domain, may inadvertently switch. A second challenge involves the field- or voltage-dependent switching response, which should be hysteretic so that a 1 or 0 state can be stored after the bit has been addressed. For solid-state materials, if the junction is sufficiently reduced in size, the hysteresis can collapse. An example is the hysteretic magnetism of ferromagnetic crystals versus the superparamagnetic response of a nanoparticle of that same material.

For our memory storage elements, we developed, with Fraser Stoddart's group, monolayers of redox-switchable,

bistable [2]rotaxane and [2]catenane molecular switches.[27,28] Such molecular switches are current- rather than field-addressed, and this removes the inadvertent switching of bits, since current only flows at the redox potentials that are characteristic of the specific molecule. In addition, we initially guessed that the switching properties would be inherently molecular in nature, and so should scale to the dimensions of a SNAP NW crossbar. This last assumption was not quite correct; the switching thermodynamics is molecule-dependent, but the kinetics depends upon the molecule and the physical environment.[29]

A SNAP-patterned, ultrahigh density 160 000 bit molecular electronic memory circuit is shown in Figure 5.[12] Four hundred Si NWs are crossed by 400 stacked insulator/metal (SiO2/ Ti) NW arrays, with all NWs patterned at 33 nm pitch. A layer of molecular switches (Figure 5B) is sandwiched in between the NWs. A major challenge associated with constructing this memory was to do as many of the fabrication steps as possible prior to deposition of the molecules and then to ensure that the molecules were protected once they were incorporated into the circuit. The completed memory was structurally perfect as measured by high-resolution scanning electron microscopy, and 100% of the NWs that were measured exhibited excellent conductivity characteristics. However, the memory itself was electronically imperfect when tested, a result that largely arose from how the various processing steps impacted the layer of molecular switches. Nevertheless, the good bits (about 25% of the total) could be configured into a read/write memory (Figure 5). The final memory circuit itself served as a compelling scientific demonstration that a working electronics circuit could be constructed at macromolecular dimensions,
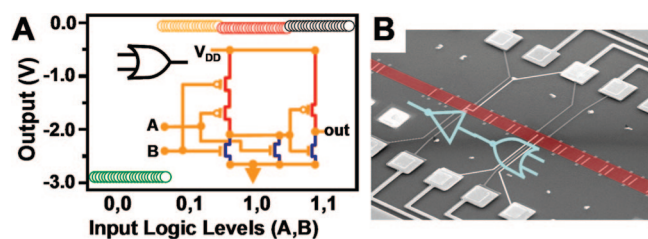
**FIGURE 6.** A complementary symmetry nanowire-based OR logic gate: (A) The measured truth table of the logic gate. For this gate, −3 V was a logic "0", and 0 V was a logic "1". As can be seen from the inset circuit diagram, the output of a NOR gate drives the input of a NOT gate. Red and blue lines within the circuit diagram highlight the p- and n-FETS, respectively. (B) A SEM micrograph of the device. A strip of 400 16 nm wide Si NWs (highlighted in red) runs diagonally across the image, and the physical location of the NOR and NOT gates are shown.

with bit densities that are more than 15 years beyond current microchip fabrication metrics.[30]

**Logic Circuits.** Building complementary symmetry (CS) NW logic circuits involves a set of challenges distinct from memory, namely, the incorporation of p- and n-type Si NW FETs into a single NW logic circuit complete with ohmic contacts and signal routing lines. Logic constitutes a more demanding NW application than does memory. For logic, the CS logic gates should exhibit gain, power efficiency, and large on/off switching ratios and the input logic voltage level should be fully restored at the output. Finally, the CS NW logic gates should have noise margins that allow for robust operation.

Many of these requirements can be addressed using the nanofabrication approaches outlined in Figure 2D and Figure 3.[16,23,31] An experimental demonstration of two-stage CS NW logic (NOR followed by NOT to produce an OR) is presented in Figure 6. A given input addresses at least one p-FET and one n-FET that are wired in series between the source voltage and ground. This is characteristic of CS logic and means that an off-state FET always shields $V_{DD}$ from ground, thus providing energy efficiency if the leakage currents are low. We investigated the properties of statistical numbers of CS logic gates, and by integrating *in silico* circuit modeling in feedback with device fabrication and testing, we demonstrated a number of key performance metrics using Si multi-NW FETs. These include full signal restoration, logic gates with a gain of 40−50, excellent noise margins, and relatively low off-currents.[13] CS NW logic gates with single-NW FETs do not exhibit such uniform performance, a result that may arise from statistical fluctuations in the numbers of dopant atoms or from their high surface-to-volume ratio.

## Materials Applications

Many advances in nanotechnology have been predicated upon physically confining systems to dimensions below characteristic length scales. Examples include the size of the exciton in a quantum dot and its influence on the optical properties of that particle. Other examples include how thermodynamic length scales can modify phase transitions[32] in nanosystems or the size-dependent scaling of van der Waals forces for controlling the assembly of nanostructures.[33]

A physical characteristic of nanostructured solids that has been relatively unexploited is that of lattice vibrations, or phonons. We turn now to two systems in which phonon physics is manifest: NW thermoelectric materials and NW quasi-1D superconductors.

**SNAP NW Thermoelectrics.** Thermoelectric efficiency is described by the dimensionless parameter $ZT = \sigma \mathbf{S}^2 T/\kappa$, where $\sigma$ and $\kappa$ are the electrical and thermal conductivities, respectively, and $\mathbf{S}$ is the thermopower (in $V \cdot K^{-1}$). Bulk Si has a ZT of 0.014; it is a lousy thermoelectric. Commercial materials exhibit a ZT approaching 1, and state of the art materials exhibit ZT values in excess of 2, although typically for only one type of conductor (e.g., n-type). For thermocooling or thermopower applications, both p- and n-type materials are needed.[21]

Both $\mathbf{S}$ and $\kappa$ can depend upon phonons. Phonons carry sound, dissipate heat, and are involved in the relaxation of excited electronic states. One opportunity with NWs is to lower $\kappa$. Bulk Si has a $\kappa$ of 140 $W \cdot m^{-1} \cdot K^{-1}$. For NWs, phonon scattering off the NW boundaries should decrease $\kappa$. Majumdar's group reported a $\kappa$ for 22 nm diameter Si NWs of ∼6 $W \cdot m^{-1} \cdot K^{-1}$ at 300 K.[34] The theoretical minimum for $\kappa$ is based upon the principal that the scattering length can get no shorter than the atomic spacing in the lattice. For Si, that value has been calculated to be about 0.99 $W \cdot m^{-1} \cdot K^{-1}$, in agreement with $\kappa$ for amorphous Si.[35]

The thermopower, $\mathbf{S}$, can have phonon ($\mathbf{S}_{ph}$) and electron contributions ($\mathbf{S}_e$). For lightly doped Si at low temperatures, $\mathbf{S}_{ph}$ is dominated by phonon drag. At low doping, the semiconductor Fermi surface is small, so momentum-conserving electron/phonon collisions (the first step toward dissipating heat) require long wavelength phonons. As these phonons carry heat through the lattice, they have the tendency to "drag" the electrons toward the cold end of the thermoelectric material, thus increasing $\mathbf{S}$. If those phonons collide with other phonons in nonmomentum-conserving (Umklapp) processes, then the affect of phonon drag is diminished, which is why phonon drag disappears at high *T*. It is worth noting that phonon drag
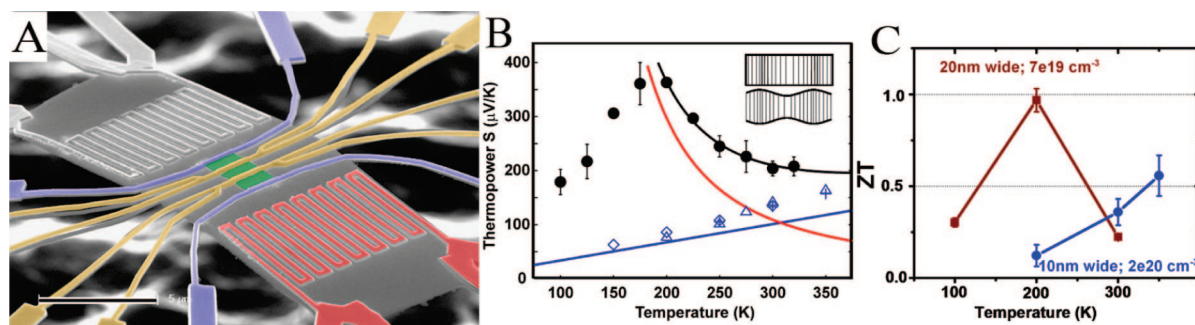
**FIGURE 7.** Si NW thermoelectrics: (A) The measurement platform (false color). The NW array is green, and the yellow electrodes are utilized for thermometry to quantify the temperature differences established with the Joule heaters (the right heater is colored red). The yellow and blue electrodes combine for four-point conductivity measurements. The gray underlying region is 150 nm thick $SiO_2$, with the underlying Si wafer etched back to suspend the platform, placing the background out of focus. (B) Thermopower calculation plotted along with experimental data (black points) from a 20 nm wide Si NW array p-type doped at $3 \times 10^{19}$ cm$^{-3}$. The black curve is the fitted expression for $S_e + S_{ph}$. The red and blue curves are $S_{ph}$ and $S_e$ from the fit. The blue data points are measured values for bulk wires (doping $2 \times 10^{20}$ cm$^{-3}$, crosses), 10 nm NWs (doping $7 \times 10^{19}$ cm$^{-3}$, diamonds), and 20 nm wires (doping $1.3 \times 10^{20}$ cm$^{-3}$, triangles) where only an $S_e$ component of $S$ was found. The drop in $S$ to 0 as $T$ approaches 0 occurs because the phonon mean free path reaches the sample size and the specific heat approaches 0 due to the third law of thermodynamics. The inset shows the character of a 3D bulk longitudinal acoustic phonon mode (top) and a 1D mode when the wavelength is larger or on the order of the NW width. The 1D mode incorporates the existence of the boundary by transverse expansion (compression) for longitudinal compression (expansion). (C) Measured ZT values for Si NWs. For the NWs represented by the red trace, $S_{ph}$ dominates $S$. $S_e$ dominates $S$ for the wires represented by the blue trace.

effects have been found to disappear in submicrometer pieces of silicon, due to surface scattering effects.[36] $S_e$, however, can be potentially enhanced in NWs due to singularities in the electronic density of states (DOS),[37] although such effects have not been experimentally observed.

The coupling of SNAP NWs onto a platform designed for the comprehensive measurements of $\sigma$, $\kappa$, and $S$ was done (Figure 7A). In Figure 7B,C, we present representative data from a number of measurements.[14] There are three remarkable observations here. First, 10 nm wide, 20 nm thick Si NWs exhibit a value of $\kappa$ ($0.76 \pm 0.15$ W·m$^{-1}$·K$^{-1}$) that is below the minimum theoretical $\kappa$ for Si. $\kappa$ would likely be further reduced for smaller NWs (based upon the observed trends).[14,38] The second observation relates to $S$. For very highly doped 20 nm wide Si NWs, $S$ is dominated by $S_e$, and is bulk-like, as expected. But for NWs doped slightly less, $S$ peaks at 200 K and appears to be dominated by $S_{ph}$, indicating the presence of phonon drag. All these Si NWs exhibit metallic-like electrical conductivity. The low values of $\kappa$ are not readily explained. However, the presence of phonon drag implies that narrow boundaries of the NWs are not providing scattering points for the long wavelength acoustic phonons; instead those phonons have become one-dimensional (Figure 7B, inset), and the relevant scattering distance is the NW length. The implication is that longer NWs should exhibit more pronounced phonon drag, a prediction that is currently being tested. The third observation is that Si NWs are high-performance thermoelectric materials!

**SNAP Quasi-1D Superconductors.** A second interesting system is that of quasi-1D superconductors. Such superconductors have diameters less than the superconducting coherence length $\xi$ and magnetic penetration depth $\lambda$. The Ginzburg–Landau order parameter $\psi$ (and the density of Cooper pairs, $|\psi|^2$) is only a function of the position $x$ along the wire.[39,40] Both $\lambda$ and $\xi$ are temperature dependent and large close to $T_c$ but quickly reduce as $T$ is reduced below $T_c$: $\xi(T) \approx \xi(0)(1 - T/T_c)^{-1/2}$ and $\lambda(T) \approx \lambda(0)[1 - (T/T_c)^4]^{-1/2}$. For pure metals, $\lambda(0)$ is ~40 nm, while $\xi(0)$ varies from ~1 $\mu$m to 40 nm.[41] Consequently, for $T < T_c$, strong quasi-1D behavior requires NWs with diameters $\ll$40 nm. In a strictly 1D system, superconductivity is not possible.[42]

Below the superconducting transition temperature, $T_c$, the electrical resistance of a bulk superconductor quickly drops to zero, while the resistance in a quasi-1D system gradually decreases to zero. This finite resistance at $T < T_c$ is a consequence of thermally activated phase slip (TAPS) and quantum phase slip (QPS) processes.[40,43,44] For TAPS, thermodynamic fluctuations (~$kT$) stochastically and instantaneously depress $|\psi|$ to zero at a random point along the wire, allowing for a sudden change of $2\pi$ in the phase of $\psi$ ("phase slip") and a finite voltage drop across the wire. TAPS and QPS processes are intrinsic to quasi-1D superconductors, and they have been studied in the low-current (i.e., small perturbation) limit in a number of systems, ranging from Nb-coated carbon nanotubes[45] to etch-thinned wires[46] and others.[47] Although these investigations have been typically plagued by
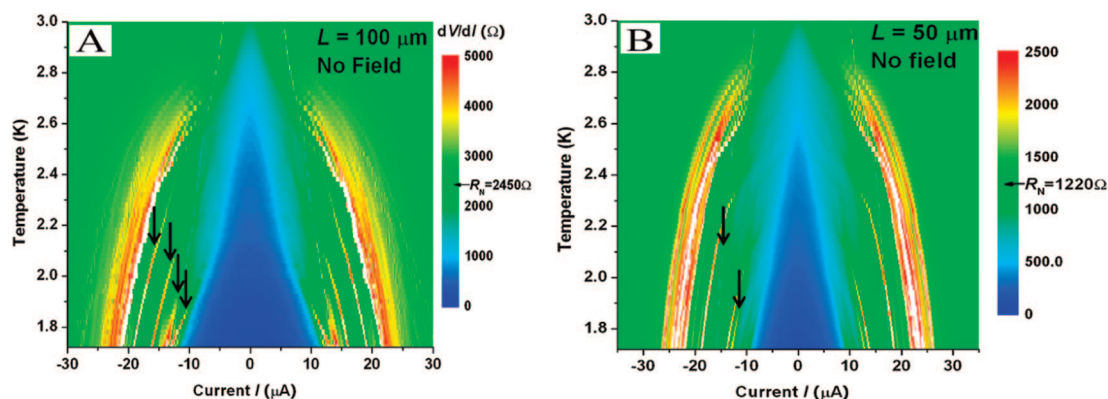
**FIGURE 8.** Phase slip centers (PSCs), indicated by arrows, in long, quasi-1D Nb NW arrays. These 100 $\mu$m (A) and 50 $\mu$m (B) long NWs are 11 nm thick and 16 nm wide. NWs 20 $\mu$m long and shorter exhibited no PSCs, indicating that $\lambda_Q^*$, the quasiparticle diffusion length, is about 12 $\mu$m. The measurement of PSCs represents a measurement of $2\lambda_Q^*$. The green color corresponds to the normal state, the blue to the superconducting state with zero measureable resistance.

issues such as proximity effects, the lack of four-point contacts, and limited materials flexibility and poor dimensional control, the studies have combined to give a fairly consistent picture.

Long NWs are more difficult to study but can exhibit additional physics in the form of localized resistance phase slip centers (PSC) along the length of the nanowires.[40] PSCs appear in the high-current limit, and each PSC occupies a characteristic length of $\sim 2\lambda_Q^*$, where $\lambda_Q^* \approx 10$ $\mu$m and is the quasiparticle diffusion length. Thus, a NW of length $L$ can accommodate $L/(2\lambda_Q^*)$ PSCs. Attempts to directly measure $\lambda_Q^*$ in true quasi-1D NWs have been limited. For example, in Sn NW arrays grown by electrodeposition, the PSCs are pinned down at local defects and are not related to $\lambda_Q^*$.[47]

The Nb NW arrays of Figure 2B are true quasi-1D superconductors.[11] By use of the monolithic fabrication approaches (Figure 2D), proximity effects were avoided, and we investigated quasi-1D superconducting physics in NWs as long as 100 $\mu$m with NW widths and thicknesses as small as 10 and 11 nm. Results relevant to the investigation of just the PSCs are shown in Figure 8, but a comprehensive picture that included TAPS and QPS processes was assimilated as well.[11] It is interesting that longer NWs are qualitatively different than short ones. Recall that, for Si NWs, phonon drag effects should make long NWs of that material fundamentally different than short NWs.

## Conclusions

The SNAP process has evolved into a tremendously versatile method that is unmatched in terms of its capability for producing high-quality nanowire arrays. The development of the SNAP process over the past few years was largely driven by the goal of developing an electronics-grade manufacturing approach that operated at macromolecular dimensions. Several benchmarks toward achieving this goal, including the fabrication of ultrahigh density memory, novel demultiplexing structures, and complementary symmetry nanowire logic circuits, have been achieved. However, the most exciting aspect of the SNAP method is that it is now allowing us to investigate and discover new physics in nanoscale materials.

## BIOGRAPHICAL INFORMATION

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## FOOTNOTES

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